Performance of GaAs on Silicon Power Amplifier for Wireless Handset Applications

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Abstract — **Recently RF devices formed by the epitaxial growth of GaAs on a Si substrate have been demonstrated [1]. The RF performance of these new devices compares well with devices on a conventional GaAs substrate process. This new GaAs-on-Si technology has the potential for replacing expensive RF components such as power amplifiers with lower cost devices fabricated on GaAs-on-Si while still maintaining good DC-RF performance. This paper presents the RF performance of these GaAs/STO/Si devices and shows for the first time their viability as power amplifiers in wireless handsets.**

I. Introduction

Over the past thirty years many researchers have attempted to grow GaAs on Si substrates with various degrees of success. Many of the challenges that arise are the high costs of growing thick epitaxial layers and the propagation of defects into active areas. These challenges have not quenched the enthusiasm of industry leaders searching for a way to combine the robustness and cost-efficiency of Si with the best properties of GaAs or other III-V materials. Recently Motorola demonstrated a way to achieve this long sought after goal by fabricating MESFETS on a GaAs/STO/Si substrate [1]. Immediately a question arises. Could these devices be utilized in existing commercial products? To answer that question we decided to implement a GaAs/STO/Si device as a power amplifier in a commercially available wireless handset. A power amplifier was chosen as the demonstration vehicle for this technology since typically, power amplifiers are one of the most critical devices in the RF chain, are more expensive and their reliability is usually lower due to their thermal operating conditions. This paper will demonstrate this technology is a viable substitute for existing RF components in wireless handsets as well as in many other items.

II. Device Description

In order to replace a commercially available power amplifier in a wireless handset, a GaAs/STO/Si device with sufficient output power capability was required. This was achieved by the fabrication of a MESFET GaAs-on-Si device with 0.7 μm gate length and 3 mm total periphery. The interested reader is referred to [1] for a more detailed description of the device structure and construction. The next step was to decide the frequency of operation for the devices. Although many of today's wireless handsets can operate in several bands, we decided to focus our attention on a single band of operation, primarily 1900 MHz. This was done in an effort to simplify and minimize required modifications to the handset itself and to better utilize the handsets available in our labs.

Accurate device data was needed in order to demonstrate that a GaAs-on-Si device is a viable substitute for a conventional power amplifier. Among the data gathered were small signal s-parameters, IV curves, load/source pull, and large signal compression curves. Furthermore, the device was characterized at several bias conditions and frequencies, including those that would be encountered when integrated into the wireless handset (3.5V battery supply, 1.9 GHz). The RF performance of these devices was measured using on-wafer ground-signal-ground probes. When biased at 3.5 V these devices exhibit a maximum stable gain of 18 dB at 1.9 GHz and an Fmax of approximately 14.5 GHz. This is shown in Figure 1 along with the performance of devices from a standard GaAs substrate. It can be seen that the data for the GaAs-on-Si devices compares very favorably with that of the conventional devices and the differences are within process variations.

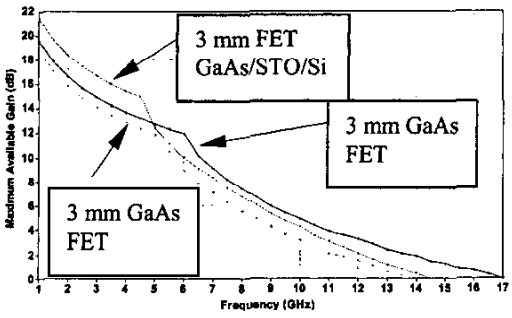

Fig. 1. Maximum Available Gain/Maximum Stable Gain of 3mm GaAs/STO/Si device and two GaAs devices for reference.

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In addition to the small signal performance, the power performance of these devices was also evaluated. Again using on-wafer ground-signal-ground probes and a Focus passive loadpull system, the optimum source and load impedances were measured. Our two tier maximum output power loadpull approach consists of first determining the source and loadpull contours of the device. A loadpull contour is shown on Figure 2 at 1.9 GHz when a GaAs/STO/Si was biased at Vds=3.5 V and Ids=207 mA.

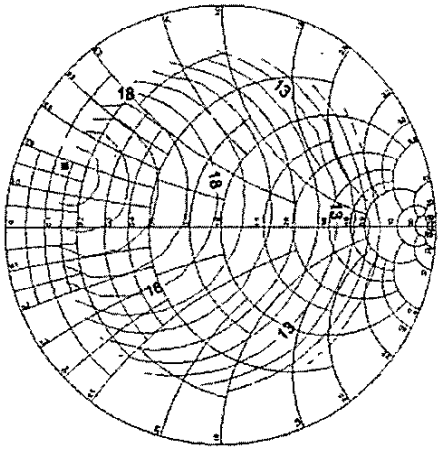

Fig. 2. Loadpull contour for 3 mm GaAs/STO/Si device biased at Vds = 3.5 V and Ids = 207 mA.

The loadpull contours provide an estimate of the source and load impedances required for maximum output power. Once these impedances have been established a more thorough peak power search is performed. This peak power search could be performed for either maximum output power (saturated) or the maximum 1-dB compression point. In this case we chose a peak power search for the maximum 1-dB compression point. During this peak power search the load and source impedances were varied around the area determined to have the optimum output power based on the loadpull contours until the maximum power had been achieved. This method is effective and efficient in determining the maximum output power of multiple devices across a wafer in a short period of time. Using this methodology the maximum output power was obtained when the load impedance was 7.8 + j12.3 Ohms. A similar source contour shows the optimum source impedance for maximum output power was 5.7 + j12.8 Ohms. When these source and load impedances were presented to the device an output power of 24.28 dBm at 1-dB compression was achieved. This represents a power density of 90 mW/mm. This power performance is shown in Figure 3.

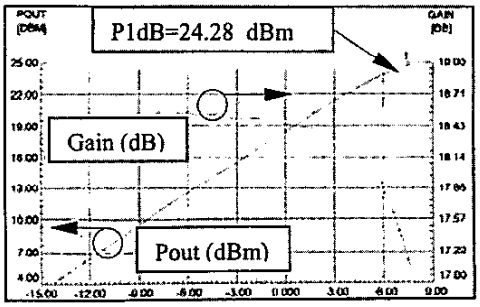

Fig. 3. Gain and output power for 3mm GaAs/STO/Si MESFET at 1.9 GHz, Vds = 3.5 V and Ids = 207 mA.

We estimated the minimum output power required to place and complete a phone call to be approximately 20 dBm. This power level, which is based solely for engineering purposes of this demonstration, does not reflect the required link margin for a commercial unit. Based on these estimates our three-millimeter devices provided enough power to demonstrate the feasibility of this technology in a commercial unit.

III. Package Considerations

The next step after characterizing the GaAs-on-Si devices was their integration in a wireless handset. Devices with a degraded performance of 20-23 dBm output power were used for this effort as test vehicles given the limited number of devices at the time. In addition, time constraints made it quite evident that minimal redesign of the package and board was necessary. For this reason, accurate models of the already existing source and load components on the PWB board, such as exciters, filters and switches were required. Transmission line elements and parasitics were also considered and analyzed with electromagnetic analysis simulation tools. Once all the components and parasitics were analyzed the source and load impedances were established at the reference plane of the packaged power amplifier. These impedances were verified by vector network analyzer measurements at the packaged amplifier footprint. This was done to ensure the impedances presented to the device itself would be mapped properly inside the package to the optimum source and load impedances as measured by the on-wafer loadpull system. The package effects were also carefully considered and analyzed since they directly affect source and load matching and can have an adverse effect on the output power of the devices.

A modified version of a TSSOP package manufactured by Amkor was used. This is the same package style the PWB was designed for and provided a drop in package with which to do the development work. The plastic

packages were modified by removing the top and center of the package, exposing the heat spreader and leads. Some preparation was needed before the GaAs/STO/Si devices could be mounted in the package. A piece of copper shim stock was soldered to the heat spreader on the bottom of the package. This supplied an additional ground connection and a thermal path when soldered to the PWB. The four corner leads were soldered to a brass carrier plate to facilitate handling and wire bonding. A thin bead of Ablebond 84-3 non-conductive epoxy was applied over the leads and cured on a hot plate to secure them in place for wire bonding. The die was attached to the heat spreader using a small amount of Ablebond 84-1 conductive epoxy and cured on a hotplate.

One problem encountered was connecting the MESFET sources to ground due to the lack of vias and the relative thickness of the die, which was 675 μm. This was solved by forming a bead of Ablebond 84-1 conductive epoxy from the heat spreader up the side and over the top of the die to the FET source pads. A chip resistor was also attached in the package to provide the gate bias. Wire bond connections were made from the package lead to the device pads paying particular attention to prevent damage to the metallization. In addition, placement of the device within the package was thoughtfully made, as it is an important factor for optimal device matching. Finally, a cover was fabricated from thin ceramic stock and attached using Ablebond 84-3. The GaAs/STO/Si power amplifier was removed from the carrier plate and installed on the PWB having the same form factor as the original PA. Figure 4 shows an internal picture of the packaged power amplifier.

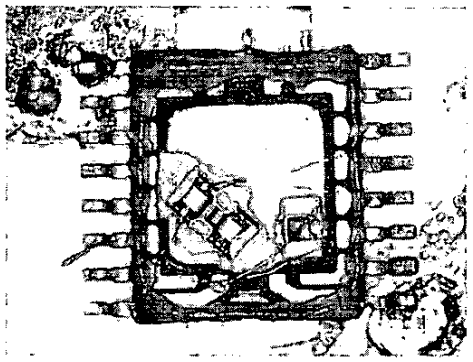

Fig. 4. Packaged power amplifier with 3 mm GaAs/STO/Si MESFET.

Figure 5 shows the optimum source and load impedances obtained by on-wafer measurements along with the load and source impedances presented to the GaAs/STO/Si device including the package, existing handset components, and modified input and output matching networks. Figure 5 shows the optimum source and load impedances presented to the device are very close to optimum. It should also be noted these impedances were obtained by selectively modifying only 7 component values on the PWB and without any additional modifications to it. This allowed for the rapid implementation of these GaAs/STO/Si devices in additional handset units.

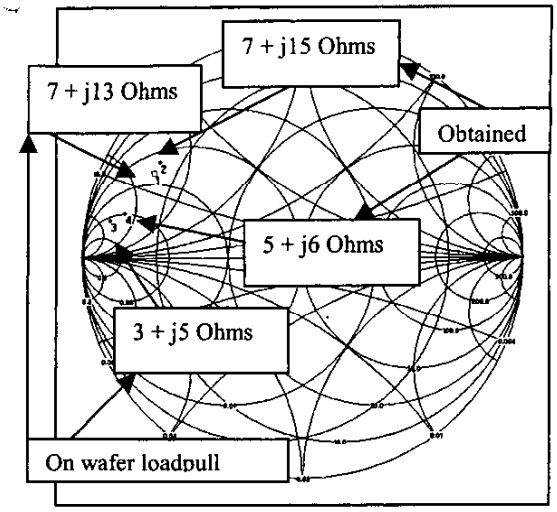

Fig. 5. On-wafer source and load impedances of 3 mm GaAs/STO/Si device and impedance obtained as implemented.

III. Handset Performance

Once the GaAs-on-Si MESFETs were integrated into Motorola Timeport handsets, a number of tests were performed. First, the RF test port was used to measure the output power of a modified phone. After compensating for the additional loss in the test port path, the output power delivered to the antenna was 19.8 dBm at 1-dB compression. This compares well with the output power obtained from on-wafer measurements ensuring the power amplifier was properly matched. As expected, 20 dBm was sufficient power to establish and complete a phone call. The first phone call was made at the Motorola Labs facility in Chandler, AZ. Additional phone calls with other handsets with GaAs/STO/Si technology were equally successful. A total of 7 handsets were built with GaAs-on-Si technology. They all exhibit similar performance. One of the handsets was used to monitor the output power level for more than 14 days continuously, with no degradation in power level.

Next, three phones were transported to Schaumburg, Illinois for additional testing. This new set of tests was designed to submit the GaAs/STO/Si powered handsets to some of the same tests commercially available units are subject to. The intent was to maximize the output power while minimizing the phase error, which affects the bit error rate. A RACAL 6103 was used for this purpose. The internal gain settings of the handsets were then optimized via software to get the optimal output power and minimum phase error. Four of the phones were then tested in the Chicago area. Multiple phone calls were established from the modified phones. In one instance a call was made by a passenger in a car, and maintained for more than 90 minutes while sightseeing around the city. The phone never dropped a call. Currently, all handsets are still operational and utilized by Motorola personnel.

IV. Conclusion

Wireless handsets that use RF power amplifiers based on a GaAs/STO/Si substrate have been fabricated. These wireless handsets represent the first time this GaAs-on-Si technology has been demonstrated in a commercial application. This technology could not only be used to reduce the cost of existing RF components such as PA and LNAs but also for developing highly integrated RF front-ends. In addition this GaAs-on-Si technology shows great potential for the optoelectronics industry.

Acknowledgement

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References

[1] K. Eisenbeiser, J. Finder, R. Emrick, S. Rockwell, J. Holmes, et. al., "RF Devices Implemented on GaAs on Si Substrates using a $SrTiO_3$ Buffer Layer," *GaAs IC Symposium.*, October 2001.